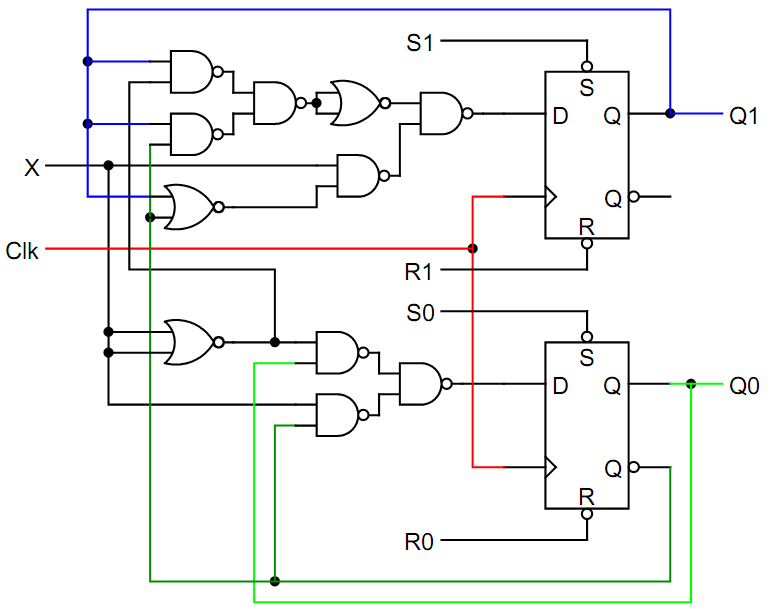
**Introduction**

The purpose of this lab was to perform an analysis of a sequential circuit, and verify it using experimental analysis. The analysis will include a derivation of the state table, state transition diagram and timing diagram.

In lab 4, this circuit diagram was given:



**Preliminary Work**

1) First, I created a wire list for the given circuit.

U1 = SN74LS00 (NAND)

U2 = SN74LS00 (NAND)

U3 = SN74LS02 (NOR)

U4 = SN74LS74A (D-Latch)

VCC 🡪 U1-14, U2-14, U3-14, U4-14, S1, S0, R1, R0

GND 🡪 U1-7, U2-7, U3-7, U4-7

X 🡪U1-12(4A),U3-?(3A),U3-?(3B),

U1-2(X1) 🡪U2-2

U2-3 (Y2) 🡪 U3-2

U2-6 (Y3) 🡪 U3-3

U2-11 (Y2) 🡪 U3-4

U3-1 (Z4) 🡪 U1-3

U1-4 (F) 🡪 LED

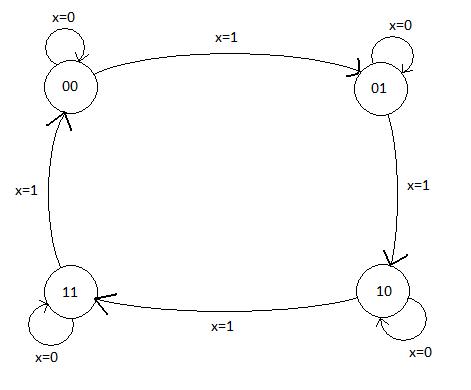
Initially S1, S0, R1, and R0 should be connected to Vcc.

2) Then I assembled the circuit

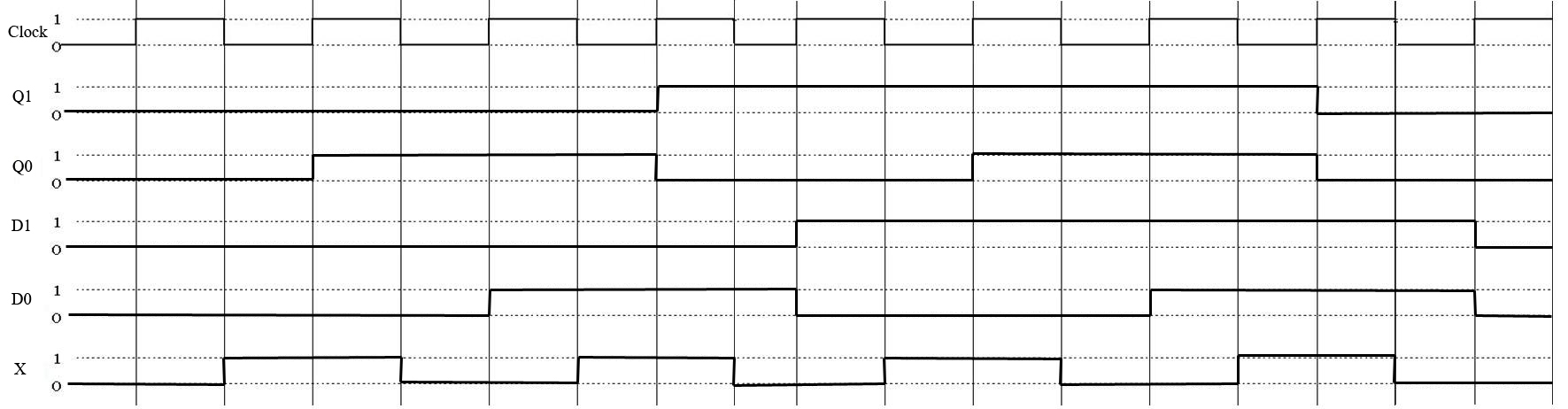
3) Then I derived the state table

|  |  |  |
| --- | --- | --- |
| Current State | X | Next State |
| 00 | 0 | 00 |
| 00 | 1 | 01 |
| 01 | 0 | 01 |
| 01 | 1 | 10 |
| 10 | 0 | 10 |
| 10 | 1 | 11 |
| 11 | 0 | 11 |
| 11 | 1 | 00 |

From the table, I created a state diagram.



4) Finally, I created a timing diagram using my wire list.



**Lab Work**

During lab 5, we tried to figure out what the circuit did. We used the following steps to accomplish this task.

1. Initialize both flip-flops to 0 with R1 and R0.

2. Describe what happens to Q1 and Q0 when X=1 for several successive clocks.

3. Use S1, S0, R1, and R0 to force each present state and clock once for X=1.

4. Use S1, S0, R1, and R0 to force each present state and clock once for X=0.

**Results**

I was not able to get any readable results from my circuit.

**Observations and Conclusions**

This was by far the largest circuit we have created and took most of the lab to finish. Making a mistake was easy, and most likely had one. From my classmates, I found out the circuit was supposed to be a 2 bit counter.